AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0026] with the following amended paragraph:

[0026] Please refer to Fig.3B with reference to Fig.3A, where Fig.3B is an equivalent circuit corresponding to the EEPROM unit depicted in Fig.3A. As shown in Fig.3B, when operated, a bit line voltage (V_{BL}) is applied to the ~~P+ doped source region 134~~ P^+ doped drain region 132 of the first PMOS transistor 101. The floating gate 122 is floating. An N-Well voltage (V_{NW}) is applied to the N-well 110. The second PMOS transistor 102 acts as a select transistor. A select gate voltage (V_{SG}) or word line voltage (V_{WL}) is applied to the select gate 124 of the second PMOS transistor 102. A source line voltage (V_{SL}) is applied to the P^+ doped source region 136 of the second PMOS transistor 102. A P-Well voltage (V_{PW}) is applied to the P-type substrate.

Please replace paragraph [0027] with the following amended paragraph:

[0027] The operation of the EEPROM according to this invention will now be described in detail with reference to an exemplary operation chart (see Fig.7), Fig.3A and Fig.3B. In Fig.7, the first (most left) column demonstrates different operation statuses including programming, reading, and erasing of the EEPROM according to this invention. The operation voltage conditions regarding writing data "1" into a selected memory cell are demonstrated in the first row of Fig.7. The operation voltage conditions regarding writing data "0" into a selected memory cell are demonstrated in the second row of Fig.7. The operation voltage conditions regarding reading data stored in memory cells are demonstrated in the third row of Fig.7. The operation voltage conditions regarding erasing data stored in memory cells are demonstrated in the fourth row of Fig.7. First, referring to the first row of Fig.7, when programming the EEPROM (writing data "1"), a relatively low-level word line voltage V_{WL} (or V_{SG}), for example, 0V, is applied to the select gate 124 of a selected EEPROM unit. A same low-level bit line voltage V_{BL} as the low-level word line voltage V_{WL}, for example, 0V, is applied to the ~~P+ doped source region 134~~ P^+ doped drain region 132 of the first PMOS transistor 101 of the selected EEPROM unit. Voltages applied to the P-type substrate 200, the N-well 110, the source line 142, and the erase gate 122 (V_{PW}, V_{NM}, V_{SL}, and V_{BG}) are 0V, 5~7V, 5~7V, and 0V, respectively. The un-selected word line is applied with a voltage ($V_{WL(un\text{-}selected)}$) having a voltage level same as V_{SL}, for example, 5~7V. The un-selected bit line is applied with a voltage ($V_{BL(un\text{-}selected)}$) having a voltage level also same as V_{SL}, for example, 5~7V. The floating gate 122 is in a floating state. As seen in the second row of Fig.7, when writing data "0" into a selected EEPROM unit, a relatively high-level bit line voltage $V_{BL(selected)}$, for example, 5~7V, is applied to the ~~P+ doped source region 134~~ P^+ doped drain region 132 of the first PMOS transistor 101 of the selected EEPROM unit.

Please replace paragraph [0031] with the following amended paragraph:

[0031] Referring to the fourth row of Fig.7 with reference to Fig.3B, when erasing the EEPROM, a relatively low-level word line voltage V_{WL} (or V_{SG}), for example, 0V, is applied. A relatively low-level bit line voltage V_{BL} of, for example, 0~5V, is applied to the ~~P+ doped source region 134~~ P+ doped drain region 132 of the first PMOS transistor 101. Voltages applied to the P-type substrate 200, the N-well 110, the source line 142 (V_{PW}, V_{NM}, V_{SL}) are a relatively low-level voltage of about 0V. A relatively high-level voltage, for example, an erase gate voltage V_{EG} =5~7V, is applied to the erase gate 120. The floating gate 122 is in a floating state. Erasing of the EEPROM unit 100 capitalizes on a so-called edge Fowler-Nordheim mechanism that occurs between the edge of the floating gate 122 and the subjacent erase gate 120. It is advantageous that at the very beginning stage of the erasing operation, electrons trapped in the floating gate 122 help to span bit line voltage (V_{BL}) through entire channel region under the floating gate, thereby facilitating the "pull-out" motion of the trapped electrons. On the other hand, as the erasing operation continues, the ejection or erasing rate of the trapped electrons slows down due to disappearing channel caused by reduced electrons in the floating gate 122. This is beneficial since no more mass of electrons at this stage is dragged out of the floating gate 122, that is, over-erase phenomenon of the EEPROM cells is avoided.

Please replace the Abstract with the following amended paragraph:

A single-poly EEPROM is disclosed. The single-poly EEPROM includes a first PMOS transistor that is serially connected to a second PMOS transistor. The first and second PMOS transistors are both formed on an N-well of a P-type substrate. The first PMOS transistor includes a floating gate, a first P^+ doped drain region, and a first P^+ doped source region. The second PMOS transistor includes a gate and second P^+ doped source region. The first P^+ doped ~~drain~~ source region of the first PMOS transistor serves as a drain of the second PMOS transistor. An erase gate extending to the floating gate for erasing the single-poly EEPROM is provided in the P-type substrate.